Amendments to the CLAIMS:

Without prejudice, this listing of the claims replaces all prior versions and listings of the claims in the present application:

LISTING OF CLAIMS:

1-15. (Canceled).

16. (Currently Amended) A method for producing a semiconductor component having a semiconductor substrate, comprising the steps of:

producing a first porous layer in the semiconductor component; and

producing one of a hollow and a cavity in the semiconductor component ~~one of~~ under ~~and from~~ the first porous layer;

wherein the one of the hollow and the cavity producing step includes the substep of producing a second porous layer having a porosity of more than approximately 70% under the first porous layer, and

wherein the one of the hollow and the cavity is produced in the one of the hollow and the cavity producing step from the second porous layer by an annealing step ~~or by an etching step with a porosity of 100%~~.

17. (Previously Presented) The method according to claim 16, wherein the semiconductor component includes a multilayer semiconductor element.

18. (Previously Presented) The method according to claim 16, wherein the semiconductor component includes a micromechanical component.

19. (Previously Presented) The method according to claim 16, wherein the semiconductor component includes a pressure sensor.

20. (Previously Presented) The method according to claim 16, wherein the semiconductor substrate includes silicon.

21. (Canceled).

22. (Currently Amended) The method according to claim [[21]] 16, wherein the second porous layer has a porosity of approximately 85% to 95%.

23. (Canceled).

24. (Previously Presented) The method according to claim 16, wherein the one of the hollow and the cavity producing step includes the substep of forming one of an access opening and a hollow open on one side in one of a direction of the first porous layer and on a second porous layer.

25. (Previously Presented) The method according to claim 24, wherein the one of the hollow and the cavity producing step includes the substep of one of partially and completely removing at least one of the first porous layer and the second porous layer via the one of the access opening and the hollow open on one side.

26. (Previously Presented) The method according to claim 16, wherein the one of the hollow and the cavity producing step includes the substep of forming an initially planar hollow under the first porous layer, the initially planar hollow increasing in depth, the one of the hollow and the cavity resulting from the initially planar hollow.

27. (Previously Presented) The method according to claim 16, wherein one of the first porous layer and the second porous layer is produced by at least one etching medium.

28. (Previously Presented) The method according to claim 27, wherein the etching medium includes hydrofluoric acid.

29. (Previously Presented) The method according to claim 27, wherein the etching medium includes at least one additive.

30. (Previously Presented) The method according to claim 29, wherein the additive includes at least one of an additive configured to reduce bubble formation, an additive configured to improve wetting and an additive configured to improve drying.

31. (Previously Presented) The method according to claim 30, wherein the additive includes an alcohol.

32. (Previously Presented) The method according to claim 31, wherein the alcohol includes ethanol.

33. (Previously Presented) The method according to claim 29, wherein a volume concentration of the additive is approximately 60% to approximately 100%.

34. (Previously Presented) The method according to claim 32, wherein a volume concentration of the ethanol is approximately 60% to approximately 100%.

35. (Currently Amended) The method according to claim 17 [[21]], wherein at least one of first porous layer and the second porous layer is produced in the respective producing step by applying an electrical field between a top and a bottom of the semiconductor element and establishing an electric current.

36. (Canceled).

37. (Previously Presented) The method according to claim 26, wherein the initially planar hollow forming step includes the substep of selecting process parameters so that one of pores and hollows of a second porous layer overlap one another in a lateral direction to form one of one single initially planar pore and one single initially planar hollow.

38. (Currently Amended) The method according to claim 27, wherein a process parameter includes at least one selected from the group consisting of a doping of the semiconductor substrate, a doping of a silicon substrate, a current density in the etching medium, a hydrofluoric acid concentration in the etching medium, at least one additive to the etching medium and a temperature.

39. (Currently Amended) The method according to claim 16, wherein said annealing step further comprises ~~further comprising~~ a high-temperature step for one of partially and completely removing hydrogen enclosed in the one of the cavity and the hollow.

40. (Previously Presented) The method according to claim 16, further comprising the step of depositing an epitaxial layer on the first porous layer.

41. (Previously Presented) The method according to claim 40, wherein the epitaxial layer includes a silicon layer.

42. (Previously Presented) The method according to claim 40, wherein the epitaxial layer includes a monocrystalline silicon layer.

43-45. (Canceled).

46-51. (Canceled).